

Listing of the Claims:

The following is a complete listing of all the claims in the application, with an indication of the status of each:

- 1 1 (Currently Amended). μ -law-to-A-law translating equipment,
2 comprising:
 - 3 a timing pulse generator that generates a reference frame pulse;
 - 4 a μ -law signal receiving circuit that receives a μ -law PCM signal
5 and outputs parallel μ -law PCM signals according to a reference frame
6 pulse, said μ -law signal receiving circuit comprising:
 - 7 a line receiver that converts the μ -law PCM signal from bipolar to
8 unipolar and outputs a unipolar μ -law signal,
 - 9 a frame buffer that temporarily stores the unipolar μ -law signal,
10 a frame detector that detects the frame leading part of the unipolar
11 μ -law signal and generates an address reset pulse
12 synchronized with the frame leading position for writing to
13 the frame buffer,
 - 14 a frame position comparator that measures the time lag in a
15 position of a reference frame pulse and the address reset
16 pulse for writing to the frame buffer and generates an
17 address reset pulse for reading from the frame buffer, and
18 a serial-parallel converter that converts and outputs a serial μ -law
19 PCM signal read from the frame buffer to parallel μ -law
20 PCM signals;
 - 21 a multiplexer that time-division multiplexes plural parallel μ -law
22 PCM signals and outputs a time-division multiplexed μ -law PCM signal;
 - 23 a μ -law-to-A-law converter that converts the time-division
24 multiplexed μ -law PCM signal to a time-division multiplexed A-law PCM
25 signal;
 - 26 a demultiplexer that demultiplexes the time-division multiplexed
27 A-law PCM signal and outputs plural parallel A-law PCM signals; and

28 an A-law signal output circuit that receives the parallel A-law PCM
29 signals and outputs a serial A-law PCM signal.

1 2 (Original). μ -law-to-A-law translating equipment according to Claim 1,
2 comprising:
3 respective plural and the same number of μ -law signal receiving
4 circuits and A-law signal output circuits.

3 (Canceled).

1 4 (Original). μ -law-to-A-law translating equipment according to Claim 1,
2 wherein:
3 the A-law signal output circuit comprises:
4 a parallel-serial converter that converts parallel A-law PCM signals
5 to a serial A-law PCM signal; and
6 a frame inserter that inserts a frame bit into the serial A-law PCM
7 signal.

1 5 (Original). μ -law-to-A-law translating equipment according to Claim 4,
2 wherein:
3 the frame inserter inserts a frame bit according to a reference frame
4 pulse.

1 6 (Original). μ -law-to-A-law translating equipment according to Claim 4,
2 wherein:
3 the A-law signal output circuit further comprises:
4 a line driver that outputs a serial A-law PCM signal at a
5 predetermined output amplitude level.

1 7 (Currently Amended). A-law-to- μ -law translating equipment,
2 comprising:

3 a timing pulse generator that generates a reference frame pulse;
4 an A-law signal receiving circuit that receives an A-law PCM
5 signal and outputs parallel A-law PCM signals according to a reference
6 frame pulse, said A-law receiving circuit comprises:
7 a line receiver that converts an A-law PCM signal from bipolar to
8 unipolar and outputs a unipolar A-law signal,
9 a frame buffer that temporarily stores the unipolar A-law signal,
10 a frame detector that detects the frame leading part of the unipolar
11 A-law signal and generates an address reset pulse
12 synchronized with the frame leading position for writing to
13 the frame buffer,
14 a frame position comparator that measures the time lag in a
15 position of a reference frame pulse and the address reset
16 pulse for writing to the frame buffer and generates an
17 address reset pulse for reading from the frame buffer, and
18 a serial-parallel converter that converts a serial A-law PCM signal
19 read from the frame buffer to parallel A-law PCM signals;
20 a multiplexer that time-division multiplexes plural parallel A-law
21 PCM signals and outputs a time-division multiplexed A-law PCM signal;
22 an A-law-to- μ -law converter that converts the time-division
23 multiplexed A-law PCM signal to a time-division multiplexed μ -law PCM
24 signal;
25 a demultiplexer that demultiplexes the time-division multiplexed
26 μ -law PCM signal and outputs plural parallel μ -law PCM signals; and
27 a μ -law signal output circuit that receives parallel μ -law PCM
28 signals and outputs a serial μ -law PCM signal.

1 8 (Original). A-law-to- μ -law translating equipment according to Claim 7,
2 comprising:
3 respective plural and the same number of A-law signal receiving
4 circuits and μ -law signal output circuits.

9 (Canceled).

1 10 (Original). A-law-to- μ -law translating equipment according to Claim 7,
2 wherein:

3 the μ -law signal output circuit comprises:
4 a parallel-serial converter that converts parallel μ -law PCM signals
5 to a serial μ -law PCM signal; and
6 a frame inserter that inserts a frame bit into the serial μ -law PCM
7 signal.

1 11. A-law-to- μ -law translating equipment according to Claim 10, wherein:
2 the frame inserter adds a frame bit to the serial μ -law PCM signal
3 according to a reference frame pulse.

1 12. A-law-to- μ -law translating equipment according to Claim 10, wherein:
2 the μ -law signal output circuit further comprises:
3 a line driver that outputs a serial μ -law PCM signal at a
4 predetermined output amplitude level.

13 (Canceled).

14 (Canceled).